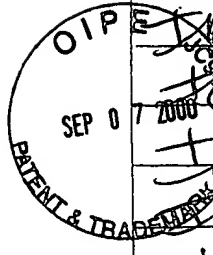


Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)	Document Number (Continuation)	Application Number
	TSmc-00-004 09/604,067	
	Applicant Ming-Dou Ker et al.	
	Filing Date	Class AT Unit
	06/26/00	

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE & APPROPRIATE
IR	5086365	2/4/92	Lien	361	58	5/8/90
IR	5631793	5/20/97	Ker et al.	361	56	9/5/95
IR	4855620	8/8/89	Duvvury et al.	307	448	11/18/87
IR	5237395	8/17/93	Lee	257	358	5/28/91
IR	5255146	10/19/93	Miller	361	56	8/29/91
IR	5287241	2/15/94	Puar	361	56	2/4/92
IR	5311391	5/10/94	Dungan et al.	361	56	5/4/93
IR	5440162	8/8/95	Worley et al.	257	355	7/26/94
IR	5610791	3/11/97	Voldman	361	56	9/6/95
IR	5625280	4/29/97	Voldman	323	284	10/30/95



FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

IR	Stephen G. Beebe, "Methodology for Layout Design and Optimization of ESD Protection Transistors, 1996 EOS/ESD Symp. Proc., pp. 265-275
IR	Polgreen et al., "Improving the ESD Failure Threshold of Silicided n-MOS Output Transistors by Ensuring Uniform Current Flow", IEEE Trans. Electron Devices, Vol. 39, pp. 379-388, 1992.

EXAMINER <i>Paul Rodriguez</i>	DATE CONSIDERED 1/8/03
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Dolichopus humilis (Cresson)

TSMC-00-004

Lighter than

09/604,067

2px²can't

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U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

IR	Duvvury et al., "Dynamic Gate Coupling of NMOS for Efficient Output ESD Protection", Proc. of IRPS, 1992, pp. 141-150.
IR	Duvvury et al., "Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability", Tech. Dig. IEDM, 1992, pp. 131-134.

EXHIBIT

Salvatore

DATE CONSIDERED

1/8/03

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Dolbe (Hummer) (C, 4)

TSMC-00-004

Lighter than sand

09/604,067

significant

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Group 27 Unit

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

IR	Ramaswamy et al., "EOS/ESD Reliability of Deep Sub-Micron NMOS Protection Devices", Proc. of IRPS, 1995, pp. 284-291.
IR	Ker et al., "Capacitor-Couple ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC", IEEE Trans, on VLSI Systems, Vol. 4, pp. 307-321, Sept. 1996.

DINNER

EXAMINER Gale A. Holsing

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1/8/03

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Dolomite (Mg, Ca)

TSMC-00-004

Ligand concentration

09 / 604,067

2x2=4

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U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

IR	Ming-Dou Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuits for Submicron CMOS VLSI", IEEE Trans. on Electron Devices, Vol. 46, No. 1, pp. 173-183, Jan. 1999.
IR	Merrill et al., "ESD Design Methodology, EOS/ESD Symp. Proc., 1994, EOS-16, pp. 141-149.

~~CLARK~~

OWNER
Rabe Raluz

DATE CONSIDERED

1/8/03

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Dashed Horizontal (Cr, 4)

TSMC-00-004

Liquidation Preference

09/604,067

Lyricism!

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U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

Dabral et al., "Core Clamps for Low Voltage Technologies, EPS/ESD Symp. Proc., 1994, EOS-16, pp. 141-149.

Worley et al., "Sub-Micron Chip ESD Protection Schemes which Avoid Avalanche Junctions", EOS/ESD Symp. Proc., 1995, EOS-17, pp. 13-20.

OLIVER

EXAMINER

Isabel Rodriguez

DATE CONSIDERED

1/8/03

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Dissolved Manganese (Crystalline)

TSMC-DO-004

High Carbon Content

09/604,067

Lycopodium

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Final Date

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Group 1st Year

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

FR	Holdman et al., "Scaling, Optimization and Design Considerations of Electrostatic Discharge Protection Circuits in CMOS Technology", EOS/ESD Symp. Proc., pp. 251-260, 1993.	
FR	Amerasekera et al., "The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design", EOS/ESD Symp. Proc., pp. 237-245, 1994.	DATE CONSIDERED 1/8/03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with communication to the applicant.

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Doctos (Hummer) (C, an)

TSMC -00-004

Signature: _____

09/604,067

significant

Ming-Dou Ker et al.

Filing Date

06/26/00

Group 21 Unit

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion(s) Pages, Etc.)

IR	Daniel et al., "Process and Design Optimization for Advanced CMOS I/O ESD Protection Devices", EOS/ESD Symp. Proc., pp. 206-213, 1990.
IR	Chen et al., "Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes", Proc. of EOS/ESD Symp., pp. 230-239, 1997.

DANGER

Isabel Dorling

DATE CONSIDERED

1/8/03

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use sword shows if necessary)

Dolores (Muriel) (Cyril)

TSMC-00-004

Ligand name

09/604,067

Application

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Filing Date

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[illegible]

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

IP	Amerasekera et al., "Substrate Triggering and Salicide Effects on ESD Performance and Protection Circuit Design in Deep Submicron CMOS Processes", IEDM Tech Digest, 1995, pp. 547-550.
IP	Anderson et al., "ESD Protection for Mixed-Voltage I/O Using NMOS Transistors Stacked in a Cascode Configuration", Proc. of EOS/ESD Symp., pp. 54-62, 1998.
EXAMINER	DATE CONSIDERED
Isabel Robles	1/8/03

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Doctor Number (Copy)

TSMC-00-004

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Application

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U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

✓	Chen et al., "Design Methodology and Optimization of
	Gate-Driven NMOS ESD Protection Circuits in Submicron
	CMOS Processes", IEEE Trans. on Electron Devices,
	Vol. 45, No. 12, pp. 2448-2456, Dec. 1998.

EXAMINEE ID:

Isabel Polanco

DATE CONSIDERED

1/8/03

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